Department: M.Tech. (VLSI and Embedded systems)			**Semester:**	**1**
Subject: VLSI Design				
Subject Code:	**24VES11**	**L – T – P - C:**		**4 – 0 – 0–4**

Sl. No	Course Objectives
1	To make the students learn the principles, operations and applications of MOSFET's.
2	To introduce the students to modelling and design of digital VLSI circuits using different CMOS design styles and CMOS sub system.
3	To make the students learn stick diagrams and layouts using Lambda based design rules for a given schematic and to categorize the different MOS Technologies

Unit	Description	Hrs
I	**MOS Transistor Theory:** n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter ,βn/βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tri state inverter, Bi CMOS inverter. (Text1)	12
II	**CMOS Process Technology Silicon Semiconductor technology:** An overview, basic CMOS technology. A basic n-well CMOS process, The p-well process, twin tub process, silicon on insulator. (Text1) **CMOS process enhancements:** Interconnect, circuit elements; Resistors, Capacitors, bipolar transistors, Thin film transistors,3DCMOS (Text1) **MOS Design Processes:** MOS layers, stick diagrams, design rules and layout, symbolic diagrams. (Text3)	10
III	**Basic circuit concepts:** Sheet resistance, standard unit of capacitance concepts, delay unit time inverter delays, driving capacitive loads, propagation delays, scaling of MOS circuits (Text3) **Basics of Digital CMOS Design:** Combinational MOS Logic circuits- Introduction, MOS logic circuits with depletion NMOS load. (Text2)	10
IV	**Basics of Digital CMOS Design: Contd..**CMOS logic circuits, complex logic circuits, CMOS Transmission Gate. (Text2) **Sequential MOS logic Circuits :** Introduction, Behavior of bi stable elements, SR latch Circuit, (Text2).	10
V	**Sequential MOS logic Circuits :Contd..** Clocked latch and Flip Flop Circuits, CMOS D- latch and triggered Flip Flop (Text2). **Dynamic CMOS and clocking:** Introduction, advantages of CMOS over NMOS, CMOS\SOS technology' CMOS\bulk technology, latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements. (Text4)	10

Course Outcomes:

Course outcome	Descriptions
CO1	Identify the different design techniques used in modeling the digital VLSI Circuits. (L1)
CO2	Estimate the parasitic values for different mask layers. (L2)
CO3	Outline the MOS process technology and CMOS sub system design. (L4)
CO4	Analyze the design parameters for the CMOS circuits. (L4)

Course Articulation Matrix

CO \ PO	PO1	PO2	PO3
CO1	2		
CO2	1		
CO3			2
CO4	2		2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Principles of CMOS VLSI Design: A System Perspective	Neil Weste and K. Eshragian,	2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
2	CMOS Digital Integrated Circuits: Analysis and Design	Sung Mo Kang &YosufLederabic Law,	3 rd edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
3	Basic VLSI Design	Douglas A. Pucknell& Kamran Eshraghian	PHI 3rd Edition (original edition 1994), 2005.
4	Introduction to VLSI Design	Eugene D Fabricius	Mc Graw Hill, International Edition (Original Edition 1990).

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	CMOS VLSI Design: A Circuits and System perspective	Neil H. E. Weste, David Harris and Ayan Banerjee	Pearson Education Pvt. Ltd.,3rd Edition,2006
2	Introduction to VLSI circuits and systems	John P Uyemura	Wiley Indian Edition,2002
3	Modern VLSI design: System on Silicon	Wayne, Wolf	Pearson Education, Second Edition.2004

SRI SIDDHARTHA INSTITUTE OF TECHNOLOGY- TUMAKURU
(A constituent College of Siddhartha Academy of Higher Education, Tumakuru)
Academic year 2024-2025

Department: M.Tech. (VLSI and Embedded systems)	**Semester:**	**1**

Subject:	**Advanced Embedded Systems**			
Subject Code:	**24VES12**		**L – T – P - C:**	**4 – 0 – 0 – 4**

Sl. No	Course Objectives
1	To make students familiar with the basic concepts of embedded systems, applications in which they are used and various aspects of embedded system design from Hardware and Software point of view.
2	To equip students with knowledge and experience of Architecture & Programming concepts of ARM microcontrollers and their supportive devices.
3	To impart an in-depth understanding of different tools and methodologies needed for the development of smart, effective and low-cost embedded system applications.
4	To make students familiar with the basic concepts of embedded systems, applications in which they are used and various aspects of embedded system design from Hardware and Software point of view.

Unit	Description	Hrs
I	**INTRODUCTION TO EMBEDDED SYSTEMS:** Evolution of microprocessors and embedded systems. General purpose computers vs Embedded systems. Performance and power consumption, Moore's law, Amdahl's law. ARM. Classifications: RISC, CISC, Flynn's Classification, Big- and little-endian CPI. Computer Architecture: Pipelining stages, Superscalar processing, Throughput and latency. **INTRODUCTION TO EMBEDDED SYSTEMS HARDWARE AND SOFTWARE:** Terminology – Gates – Timing diagram – Memory – Microprocessor buses – Direct memory access – Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency - Embedded system evolution trends – Interrupt routines in an RTOS environment.	**10**
II	**EMBEDDED NETWORKING:** Embedded Networking: Introduction, I/O Device Ports and Buses- Serial Bus communication protocols -RS232 standard – RS422 – RS485 – CAN Bus -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) -need for device drivers. **ARM ARCHITECTURE: Cortex-M3/M4 Microcontroller TM32L15xxx ARM Cortex M3/M4 Microcontroller:** Memory and Bus Architecture, Power Control, Reset and Clock Control. STM32L15xxx Peripherals: GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART.	**10**
III	**OVERVIEW OF CORTEX-M3 CORTEX-M3 BASICS:** Registers, general purpose registers, stack pointer, link register, program counter, special registers, operation mode, exceptions and interrupts, vector tables, stack memory operations, reset sequence. **Instruction Sets:** Assembly Basics, Instruction List, Instruction Descriptions. **Cortex-M3 Implementation Overview:** Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus.	**10**
IV	**CORTEX-M3/M4 PROGRAMMING:** Typical Development Flow, CMSIS (Cortex Microcontroller Software Interface Standard), Using Assembly. **Exception Programming:** Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Vector Table Relocation. **Memory Protection Unit and other Cortex-M3 features:** MPU Registers, Setting Up the MPU, Power Management, Multiprocessor Communication.	**10**
V	**Case Study and Embedded System Application Development:** Embedded system applications in home, infrastructures, buildings, security, Industries,	

	Home appliances etc. Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (ARM Cortex).	**12**

Course Outcomes:

Course outcome	Descriptions
CO1	To understand and explore various Embedded Development Strategies, Tools and Techniques available for design and development of embedded system applications.
CO2	Understand, Define, Explain and Explore Architecture & Programming of ARM microcontrollers.
CO3	Incorporate suitable microcontroller along with appropriate interfacing circuits and implement the same for an application with software programs.
CO4	Design systems based on ARM microcontroller and its interfaces.

Course Articulation Matrix

PO/PSO CO	PO1	PO2	PO3
CO1	2	1	3
CO2	2		2
CO3	2		3
CO4	-	2	3

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Embedded System-Architecture, Programming, Design	Rajkamal,	, Mc Graw Hill, 2013.
2	Embedded system Design	Peckol,	, John Wiley and Sons,2010

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Embedded Systems-An Integrated Approach,	Lyla B Das,	Pearson, 2013
2	"ARM System-on-Chip Architecture"	Steve Furber,	2nd Edition, Pearson Education
3	STM32L152xx ARM Cortex M3 Microcontroller Reference Manual	-	.

Department: M.Tech. (VLSI and Embedded systems)		**Semester:**	**1**
Subject: Advanced Digital system design with FPGA			
Subject Code:	**24VES13**	**L – T – P - C:**	**4 – 0 – 0–4**

Sl. No	Course Objectives
1	Understand the concepts of Real world circuits, Digital systems and Embedded Systems..
2	Discuss the Combinational Circuits and Sequential Circuits, its verilog code and its Verification
3	Study the Architecture of FPGA devices.
4	Learn the processor basics and I/O controllers used in embedded systems.

Unit	Description	Hrs
I	Introduction to Verilog and Design Methodology: Verilog IEEE standards, Verilog Data Types: Net, Register and Constant. Verilog Operators, Number representation and Verilog ports, Simulation and Synthesis, Test-benches. Verilog Primitives. Logic Simulation, Design Verification, and Test Methodology: Four-Value Logic and Signal Resolution in Verilog, Test Methodology Signal Generators for Test benches, Sized Numbers. Introduction to Design Methodology: Digital Systems and Embedded Systems, Real-world circuits. Design Methodology: Design Flow-Architecture, Functional design and verification.	10
II	Number Basics and Verilog Modelling Styles: Number Basics: Unsigned and Signed Integers, Fixed-point and Floating-point Numbers. Boolean Functions and Boolean Algebra, Verilog models for Boolean switching function, Binary Coding. Behavioural Modelling: Latches and Level-Sensitive Circuits in Verilog, Cyclic Behavioural Models of Flip-Flops and Latches, Behavioural Models of Multiplexers, Encoders, Decoders and Arithmetic circuits. Dataflow Modelling: Boolean Equation-Based Models of Combinational Logic, Propagation Delay and Continuous Assignments. Linear-Feedback Shift Register. Tasks & Functions. Structural Modelling: Design of Combinational Logic, Verilog Structural Models, Top-Down Design and Nested Modules.	10
III	Synthesis of Digital Sub-systems: Synthesis of Combinational Sub-systems: Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches, Synthesis of Three-state Devices and Bus Interfaces. Synthesis of Sequential Sub-systems: Synthesis of Sequential Logic with Flip-Flops, Synthesis of Explicit State Machines, Registered Logic, State Encoding, Synthesis of Implicit State Machines, Registers and Counters.	10
IV	System Implementation and Fabrics: CPLD vs FPGA Architecture - Programming Technologies-Chip I/O Programmable Logic Blocks- Fabric and Architecture of FPGA. Xilinx Virtex 5.0 Architecture , AlTERA Cyclone II Architecture	10
V	Processor Design and System Development: Design of Processor Architectures: Functional Units for Addition, Subtraction and Multiplication (overview). Interfacing Concepts: Embedded Computer Organization, Instruction and Data, Memory Interfacing. I/O Interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission.	12

Course Outcomes

Course outcome	Descriptions
CO1	Define IEEE-1364 standard and identify different styles of modelling to build digital systems.
CO2	Design and verify the digital circuits using verilog HDL at different levels of abstraction.(L3)
CO3	Identify the synthesis of combinational and sequential systems.
CO4	Outline the Concepts of FPGA Architecture and I/O Controllers used in embedded system.(L2)

Course Articulation Matrix

PO/PSO CO	PO1	PO2	PO3
CO1	2		3
CO2	3		3
CO3	3		3
CO4	3		3

Text Books:

Sl. No.	Title	Authors	Volume and Year of Edition
1.	Digital Design: An Embedded Systems Approach Using VERILOG	Peter J. Ashenden	Elsevier, 2010.
2.	Advanced Digital Design With the Verilog HDL, ,	Michael D. Ciletti	2nd Edition, 2015, PHI,
3.	Digital Systems Design Using Verilog,	Charles Roth, Lizy K. John, ByeongKil Lee	1st Edition, 2015, Cengage Learning,

Reference Book:

Sl. No.	Title	Authors	Volume and Year of Edition
1	Fundamentals of Digital Logic with Verilog Design	Stephen Brown and ZvonkoVranesic	6th Edition, 2014, McGraw Hill publication

Department: M.Tech. (VLSI and Embedded systems)			**Semester:**	**1**
Subject: Application Specific Integrated Circuits				
Subject Code:	**24VES14**	**L – T – P - C:**		**3 – 0 – 0 –3**

Sl. No	Course Objectives
1	Explain ASIC methodologies and programmable logic cells to implement a functionon IC.
2	Analyse back-end physical design flow, including partitioning, floor-planning,placement, and routing.
3	Understand the ASIC Cell library design
4	Knowledge to carry out FPGA and ASIC designs.

Unit	Description	Hrs
I	**Introduction to ASICs:** Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carryselect, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.	8
II	**ASIC Library Design:** Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multistage cells, Optimum delay and number of stages, library cell design. **Programmable ASIC:** Antifuse, Static RAM, EPROM and EEPROM Technology, FPGA, Programmable ASIC logic cells, ASIC I/O cells, Programmable ASIC Interconnects.	8
III	**Low-level design entry:** Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. **ASIC Construction:** Physical Design, CAD Tools, System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.	8
IV	**Floor planning and placement:** Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow.	8
V	**Routing**: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing – Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.	8

Course Outcomes:

Course outcome	Descriptions
CO1	Interpret the concepts of ASIC design methodology, data path elements, logical effort. (L2)
CO2	Identify and use Programmable ASIC memories according to design requirements. (L2)
CO3	Analyse the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow. (L3)
CO4	Create floor plan including partition and routing with the use of CAD algorithms. (L3)

Course Articulation Matrix

CO \ PO	PO1	PO2	PO3
CO1	3	3	
CO2	2	3	
CO3	2	3	2
CO4	2	3	2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Application - Specific Integrated Circuits	Michael John Sebastian Smith	Addison- Wesley Professional, 2003
2	VLSI Design: A Practical Guide for FPGA and ASIC Implementations	Vikram Arkalgud Chandrasetty	Springer, 2011 ISBN: 978-1-4614-1119-2.
3	An ASIC Low Power Primer	Rakesh Chadha, Bhasker J	Springer, ISBN: 978-1-4614-1119-2. 2011

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	CMOS VLSI Design: A Circuits and Systems Perspective	Neil H.E. Weste, David Harris, and Ayan Banerjee	Addison Wesley/ Pearson education 3rdedition, 2011
2	Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing	Jose E.France, YannisTsividis	Prentice Hall, 2nd Edition 1993

Department: ECE			**Semester:**	**I**
Subject: Analog and Mixed Mode VLSI Design				
Subject Code:	**24VES151**		**L – T – P - C:**	**3-0-0-3**

Sl. No	Course Objectives
1	To study the different CMOS amplifier configurations.
2	To have an insight on differential amplifiers and operational amplifiers.
3	To understand the concept of current mirrors and its types.
4	To have an insight of different oscillators and noise characteristics.

Unit	Description	Hrs
I	**CMOS Single Stage Amplifiers:** Common-Source stage (with resistive load, diode connected load, current-source load, Triode load, Source degeneration), source follower, common-gate stage.	**08**
II	**Differential Amplifier:** Single-ended and differential operation, basic differential pair – qualitative and quantitative analyses, common-mode response. **Operational Amplifiers:** Performance parameters of op-amp, one stage op-amp.	**08**
III	**Operational Amplifiers (contd.)** Two-stage CMOS op- amp. Gain boosting, Slew rate, power supply rejection. **Passive and Active Current Mirrors**: Basic Current Mirrors, Cascode and active current mirrors.	**08**
IV	**Oscillators:** General considerations, Ring oscillators, LC oscillators – cross- coupled oscillators, Colpitts oscillator, One-port oscillator and voltage-controlled oscillators.	**08**
V	**Noise Characteristics:** Statistical characteristics of noise, Types of noise - thermal noise, flicker noise, Representation of noise in circuits, noise in single- stage amplifiers (CS stage)	**07**

Course Outcomes:

Course outcome	Descriptions
CO1	Analyze different amplifier configurations. (L2)
CO2	Interpret the concepts of current mirrors. (L2)
CO3	Outline the performance of oscillator topologies. (L1)
CO4	Infer the characteristics of Noise and its types. (L2)

Course Articulation Matrix

CO \ PO	PO1	PO2	PO3
CO1	2		2
CO2	1		1
CO3	2		
CO4			2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Design of analog CMOS integrated circuits	Razavi	McGraw Hill, Edition 2002
2	CMOS Mixed Signal Circuit Design	R. Jacob Baker	Volume –II, John Wiley & Sons, INC. 2009.
3	Design of Analog CMOS Integrated Circuits	B Razavi	Tata McGraw Hill, 2009.

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Analysis and design of Analog Integrated Circuits.	Gray, Meyer, Lewis, Hurst	Willey International, 4th Edition, 2002.
2	CMOS analog circuit design.	Allen, Holberg	Oxford University Press, 2nd Edition, 2012.

Department: M.Tech. (VLSI and Embedded systems)			**Semester:**	**1**
Subject: VLSI PROCESS TECHNOLOGY				
Subject Code:	**24VES152**	**L – T – P - C:**		**3 – 0 – 0–3**

Sl. No	Course Objectives
1	To understand physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.
2	To learn the various lithography techniques and concepts of wafer exposure system.
3	To understand Concepts of thermal oxidation and deposition, ion implementation.
4	To learn concepts of dopant solid solubility, diffusion macroscopic point, metallization, process simulation and VLSI process integration.

Unit	Description	Hrs
I	**CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION:** Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, Vapour Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Thin Oxides, Oxidation Techniques and Systems, Oxide properties.	8
II	**LITHOGRAPHY AND RELATIVE PLASMA ETCHING:** Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, relative Plasma Etching techniques.	8
III	**DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALLIZATION:** Deposition process, Models of Diffusion in Solids, Flick's one Dimensional Diffusion Equation – Range Theory- Implant equipment. Annealing Shallow junction– Physical vapors Deposition – Patterning.	8
IV	**PROCESS SIMULATION AND VLSI PROCESS INTEGRATION:** Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.	8
V	**ANALYTICAL AND PACKAGING OF VLSI DEVICES:** Analytical Beams – Beams Specimen interactions – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.	7

Course Outcomes:

Course outcome	Descriptions
CO1	Appreciate the various techniques involved in the VLSI fabrication process. (L3)
CO2	Understand the different lithography methods and etching process.(L2)
CO3	Study the Epitaxy, Oxidation, depositions and diffusion mechanisms.(L1)
CO4	Understand the nuances of assembly and packaging of VLSI devices.(L2)

Course Articulation Matrix:

PO/PSO / CO	PO1	PO2	PO3
CO1	3		
CO2		1	
CO3	1		
CO4			2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	VLSI Technology	S.M.Sze	McGraw Hill, 2nd Edition. 2008.
2	ULSI Technology	C.Y. Chang & S.M.Sze	McGraw Hill,1996.
3	VLSI Fabrication Principles	S.K. Gandhi	John Wiley Inc., New York, 1994(2nd Edition)
4	Silicon VLSI Technology: fundamentals practice and Modeling	James D Plummer, Michael D. Deal, Peter B.Griffin	Prentice Hall India, 2009.

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Fundamentals of Modern VLSI Devices	Yuan Taur, Tak. H. Ning	Cambridge University Press, 2003.
2	The Science and Engineering of Microelectronic Fabrication	Stephena, Campbell	2nd edition,oxford university press, 2005.

Department: M.Tech. (VLSI and Embedded systems)		**Semester:**	**1**
Subject: Semiconductor Device Modelling			
Subject Code:	**24VES153**	**L – T – P - C:**	**3 – 0 – 0 –3**

Unit	Description	Hrs
I	Charge Carriers and Transport Modelling Crystal Structure, Semiconductor Models, Carrier Properties, State and Carrier Distributions, Equilibrium Carrier Concentrations, Drift, Diffusion, Recombination-Generation, Equations of State, Modelling & Simulation examples.	8
II	PN Junction Diodes PN Junction Electrostatics, Preliminaries, Quantitative Electrostatic Relationships, I-V Characteristics, The Ideal Diode Equation, Deviations from the Ideal, Small-Signal Admittance, Reverse-Bias Junction Capacitance, Forward-Bias Diffusion Admittance, MS Contacts and Schottky Diodes, Solar cells and LEDs.	8
III	BJT Electrostatics, Performance Parameters, Ideal Transistor Analysis, General Solution, Simplified Relationships, Ebers-Moll Equations and Model, Deviations from the Ideal, Modern BJT Structures.	8
IV	MOS Electrostatics, Capacitance-Voltage Characteristics, Quantitative ID/VD Relationships, Square-Law Theory, Bulk-Charge Theory, a.c. Response, Small-Signal Equivalent Circuits, Cutoff Frequency, Small-Signal Characteristics	8
V	Emerging electron devices (Qualitative approach): Introduction, HEMT, HBT, Fin-FET. Nanowire-FET, quantum and molecular devices, energy storage and harvesting Electronics devices	8

Course Outcomes:

Course outcome	Descriptions
CO1	Apply semiconductor models to analyse carrier densities and carrier transport.
CO2	Analyse basic governing equations to analyse semiconductor devices.
CO3	Design the p-n junction, Schottky barrier diodes and emerging semiconductor devices.
CO4	Model & simulate microelectronic devices using software tools.

Course Articulation Matrix

PO / CO	PO1	PO2	PO3
CO1	3	2	
CO2	2	3	
CO3	3	3	2
CO4	2	3	2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	"Semiconductor Device Fundamentals"	Robert F. Pierret	Pearson, 2006, ISBN 9780201543933.
2	"Operation and modelling of the MOS Transistor"	Y.P. Tsividis, Colin McAndrew	3rd Edition, 2014, Oxford Univ Press, ISBN:978-0195170153

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	"Fundamentals of Modern VLSI Devices"	Yuan Taur, Tak H. Ning	2nd edition , 2013Cambridge University Press, ISBN: 978-1107635715.
2	Semiconductor Simulation Tools	“https://nanohub.org/groups/semiconductors”	

Department: M.Tech. (VLSI and Embedded systems)		**Semester:**	2
Subject:Advanced process Architecture and Design			
Subject Code:	**24VES154**	**L – T – P - C:**	**3 – 0 – 0 – 3**

Sl. No	Course Objectives
1	Understand the state of computing and classification of parallel computers.
2	Learn about the properties of programs and networks for parallel computing.
3	Study system interconnect architectures and their components.
4	Gain knowledge of advanced processor technologies and architectures.

Unit	Description	Hrs
I	**Parallel Computer Models and Program and Network Properties:** The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers, Conditions of parallelism, Data and resource dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain size and latency, Program flow mechanisms, Control flow versus data flow, Data flow architecture, Demand-driven mechanisms, Comparisons of flow mechanisms.(Text Book 1: Chapter 2, Chapter 3)	8
II	**System Interconnect Architectures:** Network properties and routing, Static interconnection networks, Dynamic interconnection networks, Multiprocessor system interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining networks(Text Book 1: Chapter 4)	8
III	**Advanced Processors:** Advanced processor technology, Instruction-set architectures, CISC scalar processors, RISC scalar processors, Superscalar processors, VLIW architectures, Vector and symbolic processors(Text Book 1: Chapter 5)	7
IV	**Pipelining:** Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch handling techniques, branch prediction, Arithmetic pipeline design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipelines(Text Book 1: Chapter 6)	8
V	**Memory Hierarchy Design and Multiprocessor Architectures:** Memory hierarchy design - Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies. Multiprocessor architectures - Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory-based approaches, design challenges of directory protocols, memory-based directory protocols, cache-based directory protocols, protocol design tradeoffs, synchronization (Text Book 1: Chapter 7, Chapter 8)	8

Course outcome:

Course outcome	Descriptions
CO1	Understand the state of computing and classification of parallel computers.(L2)
CO2	Learn about the properties of programs and networks for parallel computing.(L2)
CO3	Study system interconnect architectures and their components.(L3)
CO4	Gain knowledge of advanced processor technologies and architectures.(L3)

Course Articulation Matrix:

PO/PSO CO	PO1	PO2	PO3
CO1	**2**	**2**	
CO2		**3**	
CO3		**2**	**1**
CO4		**2**	**2**

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Advanced Computer Architecture	Kai Hwang	TMH
2	Advance Microprocessor	Senthile	Oxford

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Computer Organization and Design	D. A. Patterson and J. L. Hennessey	Morgan Kaufmann, 2nd Ed.
2	Computer Architecture and Organization	J. P. Hayes	MGH
3	Memory Systems and Pipelined Processors	Harvey G. Cragon	Narosa Publication
4	Parallel Computers	V. Rajaraman & C. S. R. Murthy	PHI
5	Foundation of Parallel Processing	R. K. Ghose, Rajan Moona & Phalguni Gupta	Narosa Publications
6	Scalable Parallel Computers Architecture	Kai Hwang and Zu	MGH

Department: M.Tech. (VLSI and Embedded systems)	**Semester:**	**I**

Subject:	**SCRIPTING LANGUAGES FOR ELECTRONIC DESIGN AUTOMATION**			
Subject Code:	**24VES161**		**L – T – P - C:**	**3 – 0 – 0 – 3**

Sl. No	Course Objectives
1	To write the scripts in LINUX environment.
2	To study the principles of scripting languages like PERL,TCL and Python
3	Acquire the knowledge of automation using the languages like PERL,TCL and Python
4	Learn the concepts of different scripting languages for interpreting files and directories.

Unit	Description	Hrs
I	**UNIT–I: LINUX BASICS**: Introduction to LINUX, File system of Linux, General usage of Linux Kernel and Basic Commands, Linux users and group, Permissions for file, directory and users, searching a file and a directory, zipping and unzipping concepts. Text: 1.2 to 1.5.	9
II	**UNIT–II: PERL BASICS**: History and concepts of PERL – Scalar Data- Arrays and List Data – Control structures – Hashes – Basics I/O Regular Expressions – Functions- Miscellaneous control structures Text: 2.1 to 2.5.	**9**
III	**UNIT–III: TCL BASICS**: An overview of TCL and Tk-TCL languages syntax – Variables-Expressions – Lists –Control flow – Procedures –Errors and exceptions and script manipulations. Text: 2.7 to 2.9.	7
IV	**UNIT–IV: PYTHON BASICS**: Introduction to Python Basics- Using Python Interpreter – Brief tour on standard library – Control flow Tools – Data Structures – Regular expressions Text: 3.1 to 3.5.	7
V	**UNIT–V: ADVANCED TOPICS IN PYTHON**: Input and Output - Errors and Exceptions – Classes – Modules – Applications of Python scripts to Electronic Design Automation Text: 3.6 to 3.8.	7

Course Outcomes:

Course outcome	Descriptions
CO1	Apply commands in LINUX environments (L2).
CO2	Apply and execute PERL scripts (L2).
CO3	Use TCL scripts for automation.(L3).
CO4	Make use of Python Scripts to interpret files and directories.(L3).

Course Articulation Matrix

PO/PSO / CO	PO1	PO2	PO3
CO1	2		3
CO2	2		3
CO3	3		2
CO4	3		

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	The Linux Command Line: A Complete Introduction	William E. Shotts	2nd edition, 2019, William Pollock
2	TCL and TK Toolkit	Ken Jones	2nd edition, 2010, Pearson Education
3	Let Us Python	Yashavanth Kanetkar	6th edition, 2021, bpb Publication

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	How Linux Works	Brian Ward	3rd Edition,2020,William Pollock
2	Principles TCL and TK toolkit	John K Outsertout	3rd Edition, 2011, Pearson Education
3	Think Python	Allen B Downey	4th Edition,2020, O'Reilly Publications

Department: M.Tech. (VLSI and Embedded systems)	**Semester:**	**I**

Subject: Nano Electronics				
Subject Code:	**24VES162**		**L – T – P - C:**	**3 – 0 – 0 -- 3**

Sl. No	Course Objectives
1	To Introduce the fundamental principles and theories underlying nanoelectronics and nanoscale devices.
2	To understand the fabrication techniques and material properties essential for nanoelectronics.
3	To learn about various nanoelectronic devices, their design, and their applications and to explore the current trends and future directions in nanoelectronics.

Unit	Description	Hrs
I	**Introduction to Nanoelectronics** Foundational aspects of nanoelectronics, Classification of nanostructures and examines the electronic properties of atoms and solids, Effects of the nanometer length scale and introduces both top-down and bottom-up fabrication methods (Text Book 1: Chapter 1,2,3)	07
II	**Characterization Techniques** Techniques used to characterize nanomaterials and nanostructures, Diffraction techniques for bulk and surface analysis, Spectroscopy techniques that use photons, radiofrequency, and electrons, Reflectometry and methods for measuring the mechanical, electronic, magnetic, and thermal properties of nanomaterials. (Textbook 1: Chapter 4,5).	08
III	**Nanostructures and Carbon Nanotechnology** Inorganic semiconductor nanostructures and the physics underlying them. Quantum confinement in structures like quantum wells, wires, and dots, along with super-lattices, band offsets, and electronic density of states. Carbon nanostructures, including carbon molecules, clusters, and nanotubes, and examines their applications in various fields. (Textbook 1: Chapter 6, Text Book 2: Chapter 3).	08
IV	**Fabrication Techniques and Physical Processes** Techniques used for fabricating semiconductor nanostructures. Strain-induced and electrostatically induced dots and wires, quantum well fluctuations, and thermally annealed quantum wells. Semiconductor nanocrystals, colloidal quantum dots, and self-assembly techniques. The physical processes in these structures, such as modulation doping, quantum Hall effect, resonant tunneling, ballistic carrier transport, light emission processes, and the characterization of these nanostructures. (Text Book 1: Chapter 7,8,9).	08

V	**Applications and Advanced Topics** Advanced measurement methods and applications of nanoelectronics. Applications discussed include injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, Coulomb blockade devices, photonic structures, quantum well infrared photo detectors (QWIPs), nanoelectromechanical systems (NEMS), and microelectromechanical systems (MEMS). (Text Book 1: Chapter 10, Text Book 2: Chapter 4).	08

Course Outcomes:

Course outcome	Descriptions
CO1	Understand the basic principles and theories underlying nanoelectronics and nanoscale devices (L1).
CO2	Comprehend and explain the fabrication techniques and material properties essential for nanoelectronics (L2).
CO3	Articulate the design and working principles of various nanoelectronic devices and their applications (L3).
CO4	Evaluate the current trends and potential future directions in the field of nanoelectronics (L4).

Course Articulation Matrix:

PO/PSO / CO	PO1	PO2	PO3
CO1	**3**	**1**	**3**
CO2	**2**	**2**	**2**
CO3	**2**	**3**	**3**
CO4	**3**	**2**	**3**

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Nanoelectronics and Information Technology	Rainer Waser	Wiley-VCH, 3rd Edition, 2012
2	Introduction to Nanoscale Science and Technology	Massimiliano Di Ventra, Stephane Evoy, James R. Heflin	Springer © 2004
3	Handbook of Nanophysics: Nanoelectronics and Nanophotonics	Klaus D. Sattler	CRC Press, 2010

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	"Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications"	Vladimir V. Mitin, Viatcheslav A. Kochelap, and Michael A. Stroscio	Cambridge University Press, 2008
2	“Nano Technology : Principles and Practices”	Sulabha K Kulkarni	Springer © 2015 (3rd Edition)

Semester I **Subject Name: High Speed VLSI Design**

Subject Code: 24 VES163 **L – T – P – C: 3-0-0-3**

Course Objectives:

Course outcome	Descriptions
CO1	Apply the concepts and laws of logic design to solve logical problems(L3)
CO2	Solve complexity of logical equation using simplification techniques and decomposition methods(L4)
CO3	Design logical circuits such as encoder, decoder, sine wave.(L3)
CO4	Test the digital circuit for faults and design fault free circuit(L3)

Course Outcomes

Course Outcome	Descriptions
CO1	Study of front-end -of-line variability considerations, charge loss mechanisms, back-end-of- line variability considerations. (L1)
CO2	Design of single and dual-rail domino, and latched domino structures. (L4)
CO3	Circuit Design margin and design variability. (L2)
CO4	Study of Latching Strategies, Interface Techniques, Clocking styles. (L2)

SYLLABUS

UNIT	Description	Hours
I	**Unit 1: Process Variability:** Introduction, Front-end -of-line variability considerations, charge loss mechanisms, back-end-of- line variability considerations..	08
II	**Unit 2: Non-Clocked logic styles:** Introduction, static CMOS structures, DC VS logic, Non-clocked pass-gate families. **Clocked logic styles:** Introduction, single-rail domino logic styles. Dual-rail domino structures, latched domino structures.	08
III	**Unit 3: Circuit Design margin and design variability:** Introduction, process induced variation, design induced variations, and application induced variations, Noise. Introduction, basic latch design, latching single ended logic. **Latching Strategy:** latching differential logic.	08
IV	**Unit 4: Interface Techniques:** Introduction, signalling standard, chip-chip communication networks, ESD protection, Driver design techniques, receiver design techniques.	08
V	**Unit 5:Clocking styles:** Introduction, clock jitter and skew, clock generation and clock distribution.	07

Course Articulation Matrix

PO / CO	PO1	PO2	PO3
CO1	3		2
CO2	3	2	
CO3	2	1	3
CO4	3		1

Text Books:

Sl No	Title	Authors	Volume and Year of Edition
1	High Speed CMOS Design Styles	Kerry Bernstein & et. al.,	Kluwer, 1999
2	High Speed Digital Design	Howard Johnson & Martin Graham	A Handbook of Black Magic, Prentice Hall PTR, 1993

Reference Books:

Sl No	Title	Authors	Volume and Year of Edition
1	Digital Systems Engineering	William S. Dally & John W. Poulton	Cambridge University Press, 1998.
2	High Speed Digital Circuits	Masakazu Shoji	Addison Wesley Publishing Company, 1996.

Department: M.Tech. (VLSI and Embedded systems)	**Semester:**	**I**

Subject:	**Reconfigurable Computing**			
Subject Code:	**24VES164**		**L – T – P - C:**	**3 – 0 – 0 -- 3**

Sl. No	Course Objectives
1	To offer an introduction in the theory and engineering design principles of the modern Reconfigurable Computing Systems (RCS).
2	To give importance in understanding the concepts of architecture re-configurability, programmable logic devices and optimization of the RCS architecture.
3	To emphasis on Reconfigurable Computing Architectures and to learn languages and compilers for the RCS.

Unit	Description	Hrs
I	**Reconfigurable Computing Hardware** Device Architecture, Reconfigurable Computing Architectures, Reconfigurable Computing Systems, Reconfiguration Management. (Text Book 1: Chapter 1,2,3,4)	07
II	**Programming Reconfigurable Systems** Compute Models and System Architectures, Programming FPGA Applications in VHDL, Compiling C for Spatial Computing, Stream Computations Organized for Reconfigurable Execution, Programming Data Parallel FPGA Applications Using the SIMD/Vector Model, Operating System Support for Reconfigurable Computing (Textbook 1, Chapter 5,6,7, Textbook 2, Chapter 6,7, Text Book 3, Chapter 2,3).	08
III	**Mapping Designs to Reconfigurable Platforms** Technology Mapping, FPGA Placement, Placement for General-purpose FPGAs, Data-path Composition, Specifying Circuit Layout on FPGAs, Retiming, Re-pipelining, and C-slow Retiming, Configuration Bit-stream Generation, Fast Compilation Techniques (Textbook 1 , Chapter 13, 14, 19, Text Book 2, Chapter 2, 7).	08
IV	**Application Development** Implementing Applications with FPGAs, Instance-specific Design, Precision Analysis for Fixed point Computation, Distributed Arithmetic, CORDIC Architectures for FPGA Computing, Hardware/Software Partitioning (Text Book 1, Chapter 21, 22, 23, 24,25, 26, Textbook 2, Chapter 3,Textbook 3, Chapter 13, 17).	08
V	**Case Studies of FPGA Applications** SPIHT Image Compression, Automatic Target Recognition Systems on Reconfigurable Devices, Boolean Satisfiability: Creating Solvers Optimized for Specific Problem Instances, Multi-FPGA Systems: Logic Emulation, Finite Difference Time Domain: A Case Study Using FPGAs, Network Packet Processing in Reconfigurable Hardware (Text Book 1, Chapter 27,28,29,30).	08

Course Outcomes:

Course outcome	Descriptions
CO1	Understand the basics of the reconfigurable computing and reconfigurable architectures (L1).
CO2	Articulate the design issues involved in reconfigurable computing systems with a specific focus on FPGAs both in theoretical and application levels (L4).
CO3	Understand the performance trade-offs involved in designing a reconfigurable computing platform (L4).
CO4	Understand both how to architect reconfigurable systems and how to utilize them for solving challenging computational problems (L4).

Course Articulation Matrix:

PO/PSO CO	PO1	PO2	PO3
CO1	2		
CO2	2		2
CO3			2
CO4	1		

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Reconfigurable Computing – The Theory and Practice of FPGA-based Computation	Scott Hauck and Andre DeHon	ELSEVIER, 2008
2	Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications	Christophe Bobda	Springer © 2007
3	New Algorithms, Architectures and Applications for Reconfigurable Computing	Patrick Lysaght and Wolfgang Rosenstiel	Springer © 2005

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Embedded Systems Design with FPGAs	Peter Athanas, Dionisios Pnevmatikatos, and Walid A. Najjar	Springer © 2013.
2	VLSI: Integrated Systems on Silicon	Jürgen Becker, Marcelo Lubaszewski, and Robert Reis	Springer © 2014

SRI SIDDHARTHA INSTITUTE OF TECHNOLOGY- TUMAKURU
(A constituent College of Siddhartha Academy of Higher Education, Tumakuru)
Academic year 2024-2025

Department: M.Tech. (VLSI and Embedded systems)		**Semester:**	**I**
Subject: Digital System Design & Embedded Systems Lab			
Subject Code:	**24VESLB1**	**L – T – P - C:**	**0 – 0 – 3–1.5**

Sl. No	Course Objectives
1	Discuss the Combinational Circuits and Sequential Circuits, its Verilog code, and its Verification.
2	Interface and program peripherals with the LPC2128 microcontroller.
3	Understand the implementation of embedded systems with practical experiments.
4	Develop skills in writing and debugging embedded C programs for real-time applications.

Unit	Description	Hrs
1.	4-bit binary up/down/up-down counter with synchronous reset, BCD counter.	
2.	Sequential block to detect a sequence (say 11101) using appropriate FSM	
3.	8-bit ripple carry adder and carry skip adder	
4.	8--bit carry select adder	
5.	Generate the waveforms using DAC interface.	
6.	Interface a 16x2 LCD with the LPC2128 microcontroller and display a string of text.	
7.	Interface a 4x4 keypad with the LPC2128 microcontroller and display the pressed key on the LCD.	
8.	Generate a square wave using the Timer of the LPC2128 microcontroller.	
9.	Toggle an LED on and off using an external interrupt triggered by a push-button	
10.	Demonstrate the use of the Watchdog Timer to reset the LPC2128 microcontroller.	

Course outcome:

Course outcome	Descriptions
CO1	Discuss and verify combinational and sequential circuits using Verilog. (L2)
CO2	Develop and test embedded systems interfaced with various peripherals. (L3)
CO3	Utilize microcontroller features such as Timers, Interrupts, and Watchdog Timers in embedded applications. (L3)
CO4	Demonstrate proficiency in writing and debugging embedded C programs. (L3)

Course Articulation Matrix:

PO/PSO CO	PO1	PO2	PO3
CO1	2	2	3
CO2	2	2	3
CO3	2	2	3
CO4	2	2	3

Text Books:

Sl. No.	Title	Authors	Volume and Year of Edition
4.	Digital Design: An Embedded Systems Approach Using VERILOG	Peter J. Ashenden	Elsevier, 2010.
5.	ARM LPC2148 Based Embedded Systems: Concepts, Designs, and Programming	Sumit Ahuja	Khanna Publishers, 1st Edition, 2018
6.	Embedded Systems: Using Assembly and C	Muhammad Ali Mazidi, Shujen Chen, Sepehr Naimi	Pearson Education, 1st Edition, 2009

Reference Books:

Sl. No.	**Title**	**Authors**	**Volume and Year of Edition**
1.	Digital Design: An Embedded Systems Approach Using VERILOG	Peter J. Ashenden	Elsevier, 2010.
2.	ARM LPC2148 Based Embedded Systems: Concepts, Designs, and Programming	Sumit Ahuja	Khanna Publishers, 1st Edition, 2018.
3.	Embedded Systems: Using Assembly and C	Muhammad Ali Mazidi, Shujen Chen, Sepehr Naimi	Pearson Education, 1st Edition, 2009.
4.	Digital VLSI Design with Verilog: A Textbook from Silicon Valley Polytechnic Institute	John Williams	Springer, 2nd Edition, 2014.
5.	Embedded Systems Design: An Introduction to Processes, Tools, and Techniques	Arnold S. Berger	CMP Books, 1st Edition, 2001.

Department: M.Tech. (VLSI and Embedded systems)			**Semester:**	**2**
Subject: VLSI PHYSICAL DESIGN				
Subject Code:	**24VES21**	**L – T – P - C:**		**4 – 0 – 0–4**

Sl. No	Course Objectives
1	Able to acquire knowledge on fundamentals of VLSI technology, rules of layout, partitioning, floor planning, placement and routing algorithms.
2	Acquire knowledge of delays in gates and interconnects, single layer& multichip module routing and compaction techniques.

Unit	Description	Hrs
I	**INTRODUCTION TO VLSI TECHNOLOGY:** Layout Rules and Circuit abstraction ,Cell generation using programmable logic array, transistor chaining ,Wein Berger arrays and gate matrices , Layout Environments -layout of standard cells ,gate arrays and sea of gates, Field Programmable Gate Array (FPGA) ,layout methodologies Packaging ,Computational Complexity .	12
II	**PLACEMENT USING TOP-DOWN APPROACH**: Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan - Lin Heuristic, Ratio cut, partition with capacity and I/O constraints. Floor planning: Rectangular dual floor planning, hierarchical approach, simulated annealing, Floor plan sizing. Placement: Cost function, force directed method, placement by simulated annealing, partitioning placement, module placement on a resistive network ,regular placement linear placement.	10
III	**ROUTING USING TOP DOWN APPROACH:** Fundamentals: Maze Running, line searching, Steiner trees, Global Routing: Sequential Approaches, hierarchical approaches, multi commodity flow based techniques, Randomized Routing, One Step approach, Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA ,Row based FPGAs.	10
IV	**PERFORMANCE ISSUES IN CIRCUIT LAYOUT:** Delay Models: Gate Delay Models, Models for interconnected Delay, Delay in RC trees. Timing Driven Placement: Zero Stack Algorithm, Weight based placement, Linear Programming Approach, Timing riving Routing: Delay Minimization, Click Skew Problem, Buffered Clock Trees, Minimization: constrained via Minimization, unconstrained via Minimization.	10
V	**SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION:** Planar subset problem (PSP) , Single Layer Global Routing, Single Layer detailed Routing , Wire length and bend minimization technique ,Over The Cell (OTC) Routing ,Multiple chip modules (MCM) ,programmable Logic Arrays , Transistor chaining , Wein Burger Arrays and Gate matrix layout , 1D compaction , 2D compaction.	10

Course Outcomes:

Course outcome	Descriptions
CO1	Understand the concepts of partitioning, floor planning, placement and routing of the cells as per the layout rules using the top down approach.
CO2	Interpret on delay modelling, delay minimization with respect to physical design.
CO3	Outline single layer and over the cell routing and apply 1D and 2D compaction techniques

Course Articulation Matrix:

PO/PSO / CO	PO1	PO2	PO3
CO1	3		
CO2		1	
CO3			2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	"An Introduction to VLSI Physical Design"	Majid Sarrafzadeh, C. K. Wong,	McGraw Hill, 1996
2	"Physical Design and Automation of VLSI systems"	Preas M. Lorenzatti,	The Benjamin Cummins Publishers, 1998.
3	"VLSI Physical Design Automation: Theory and Practice",	Sadiq M. Sait, Habib Youssef,	World Scientific Publishers, 1999.

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	"Practical Problems in VLSI Physical Design Automation",	Sung Kyu Lim,	Springer Publications,2008.
2	"VLSI Physical Design: From Graph Partitioning to Timing Closure",	Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu	Springer Publications, 2011
3	"Introduction to VLSI Circuits and Systems",	John P. Uyemura,	John Wiley and Sons, 2002

Department: M.Tech. (VLSI and Embedded systems)		**Semester:**	**2**
Subject: Advanced VLSI Design			
Subject Code:	**24VES22**	**L – T – P - C:**	**4 – 0 – 0–4**

Sl. No	Course Objectives
1	To make the students to learn the principles, operations and quantitative analysis of the semiconductor devices MESFETs, MODFETs and MOSFETs.
2	Realize the stick diagrams and layouts using Lambda based design rules for a given schematic and to categorize the different MOS technologies.
3	To make the students to learn special circuit layouts and technology mapping and system design.

Unit	Description	Hrs
I	**Review of MOS Circuits:** More Moore and more- than More Moore **MESFETS:** MESFET and MODFET operations, quantitative description of MESFETS. (Text1).	12
II	**MIS Structures and MOSFETS:** MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS. (Text1)	10
III	**Short Channel Effects and Challenges to CMOS:** Short channel effects, scaling theory, processing challenges to further CMOS miniaturization **Beyond CMOS:** Evolutionary advances beyond CMOS, carbon Nano tubes. (Text1).	10
IV	**BeyondCMOS:** Conventional vs. tactile computing, computing, molecular and bio-logical computing Mole electronics-molecular Diode and diode- diode logic, Defect tolerant computing, Quantum dot cellular automata. (Text1). System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic. (Text2).(Text Book 2: 6.1, 6.2, 6.3.1,6.3.2,6.3.3, 8.2, 8.3)	10
V	**System Design:** Contd.. Programmable inter connect, programmable structure, Gate arrays standard cell approach. (Text2). **Special Circuit Layouts and Technology Mapping:** Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter. (Text3)	10

Course Outcomes:

Course outcome	Descriptions
CO1	Analyze transistor level schematics, scaling parameters and outline the various fabrication processes. (L2)
CO2	Estimate the design parameters for speed, area and power optimization. (L3)
CO3	Apply the different design techniques used in modeling the digital circuits. (L3)
CO4	Design the sub systems using different CMOS design styles. (L4)

Course Articulation Matrix

CO \ PO	PO1	PO2	PO3
CO1	2		
CO2		1	
CO3		2	2
CO4	2		2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Introduction to Semi-Conductor Devices	Kevin F Brennan	Cambridge publications. 2nd Edition 2008
2	Principles of CMOS VLSI Design: A System Perspective	Neil Weste and K. Eshragian,	Pearson Education (Asia) Pte. Ltd., 2nd edition, 2000.
3	Introduction to VLSI Design	Eugene D Fabricius	Mc Graw Hill, Interna-tional Edition (Original Edition 1990).

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	CMOS VLSI Design: A circuits and Systems Perspective	Neil H. E. Weste, David Harris and Ayan Banerjee	Pearson Education Pvt. Ltd.,3rd Edition,2006
2	Fundamentals of Semiconductor Devices	M. K. Achuthan and K.N. Bhat	Tata McGraw-Hill, 2nd Edition,2006
3	CMOS Digital Integrated Circuits: Analysis and Design	Sung-Mo Kang & Yusuf Leblebici	Tata McGraw-Hill 3rd Edition,2003
4	Modern VLSI Design- IP Based Design	Wayne Wolf	PHI Publishers, 4th Edition,2009

Department: M.Tech. (VLSI and Embedded systems)	**Semester:**	**2**

Subject: Real Time Embedded Systems				
Subject Code:	**24VES23**		**L – T – P - C:**	**4 – 0 – 0 – 4**

Sl. No	Course Objectives
1	Introduce the fundamental concepts of Real Time Operating Systems and the real time embedded system
2	Apply concepts relating to operating systems such as Scheduling techniques, Thread Safe Reentrant Functions, Dynamic priority policies.
3	Describe concepts related to Multi resource services like blocking, Deadlock, live lock & soft real-time services.
4	Discuss Memory management concepts, Embedded system components, Debugging components and file system components.

Unit	Description	Hrs
I	**Arm Processor And Peripherals** ARM Architecture Versions – ARM Architecture – Instruction Set – Stacks and Subroutines – Features of the LPC 214X Family – Peripherals – The Timer Unit – Pulse Width Modulation Unit – UART – Block Diagram of ARM9 and ARM Cortex M3 MCU.	**10**
II	**Real-Time Systems and Resources**: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions. (Text 1: Selected sections from Chap. 1, 2)	**10**
III	**Processing with Real Time Scheduling**: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy. (Text 1: Chap. 2,3,7)	**10**
IV	**Memory and I/O**: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software. (Text 1: Selected topics from Chap. 4,5,6,7,11).	**10**
V	**Firmware Components**: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, Checking return codes, Single-step debugging, Test access ports, Trace Ports. (Text 1: Selected topics	**12**

Course Outcomes:

Course outcome	Descriptions
CO1	Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities, debugging methodologies and optimization techniques.
CO2	Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/FPGA/ASIC to improve the system performance.
CO3	Apply priority based static and dynamic real time scheduling techniques for the given specifications.
CO4	Analyze deadlock conditions, shared memory problem, critical section problem, missed deadlines, availability, reliability and QoS.

Course Articulation Matrix

PO/PSO CO	PO1	PO2	PO3
CO1	2	1	3
CO2	2		2
CO3	2		3
CO4	-	2	3

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Embedded System-Architecture, Programming, Design	Rajkamal,	Mc Graw Hill, 2013.
2	"Real-Time Embedded Systems and Components",	Sam Siewert,	Cengage Learning India Edition, 2007.
3	Embedded/Real Time Systems, Concepts, Design and Programming, Black Book,	Dr. K.V.K.K Prasad	Dream Tech Press, New edition, 2010.

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	"Real Time System", 2.	James W S Liu	Pearson education, 2008.
2	"Programming for Embedded Systems",	Dream Tech Software Team,	John Wiley, India Pvt. Ltd., 2008.

Department: M.Tech. (VLSI and Embedded systems)		**Semester:**	2
Subject: SYSTEM VERILOG FOR DESIGN AND VERIFICATION			
Subject Code:	**24VES24**	**L – T – P - C:**	**4 – 0 – 0 – 4**

Sl. No	**Course Objectives**
1	Understand the concepts of verification methodologies and data types.
2	Learn the procedural statements, routines, and assertions in SystemVerilog.
3	Study the Object-Oriented Programming (OOP) concepts in SystemVerilog.
4	Acquire knowledge on randomization and functional coverage in SystemVerilog.

Unit	**Description**	**Hrs**
I	**Verification Guidelines and Data Types:** Verification Guidelines: Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Test Bench Components, Layered Test Bench, Building Layered Test Bench, Simulation Environment Phases, Maximum Code Reuse, Test Bench Performance. Data Types: Built-in Data Types, Fixed-size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing a Storage Type, Creating New Types with typedef, Creating User-defined Structures, Type Conversion, Enumerated Types, Constants, Strings, Expression Width. (Text1:Chapter 2 and 3)	11
II	**Routines and Connecting the Test Bench & Design:** Procedural Statements and Routines: Procedural Statements, Tasks, Functions and Void Functions, Routine Arguments, Returning from Routine, Local Data Storage, Time Values. Connecting the Test Bench and Design: Separating the Test Bench and Design, Interface Constructs, Stimulus Timing, Interface Driving and Sampling, Connecting It All Together, Top-Level Scope, Program – Module Interactions, SystemVerilog Assertions. (Text1:Chapter 4 and 5)	10
III	**Basic OOP:** IIntroduction: First Class, Define a Class, OOP (Object-Oriented Programming) Terminology, Creating New Objects, Object De-allocation, Using Objects, Static Variables vs. Global Variables, Class Methods, Defining Methods Outside of the Class, Scoping Rules, Using One Class Inside Another, Understanding Dynamic Objects, Copying Objects, Public vs. Private, Straying Off Course, Building a Test Bench. (Text1: Chapter 6)	10
IV	**Randomization:** ntroduction: Randomization, Randomization in SystemVerilog, Constraint Details, Solution Probabilities, Controlling Multiple Constraint Blocks, Valid Constraints, In-line Constraints, The pre_randomize and post_randomize Functions, Constraints Tips and Techniques, Common Randomization Problems. (Text1:Chapter 7)	10
V	**Interprocess Communication and Functional Coverage :** Interprocess Communication: Events, Semaphores, Mailboxes. Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of a Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, Measuring Coverage Statistics During Simulation. (Text1:Chapter 8 and 9)	11

Course outcome:

Course outcome	Descriptions
CO1	Understand the concepts of verification methodologies and data types. (L2)
CO2	Summarize the concepts of procedural statements, routines, and assertions. (L2)
CO3	Illustrate the concepts of OOP terminology. (L3)
CO4	Demonstrate the randomization in SystemVerilog. (L3)

Course Articulation Matrix:

PO/PSO CO	PO1	PO2	PO3
CO1	2	2	
CO2		3	
CO3		2	1
CO4		2	2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	SystemVerilog for Verification	Chris Spears	Springer, 2nd Edition, 2008

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	A Practical Guide for SystemVerilog Assertions	Vijayaraghavan, Srikanth, and Meyyappan Ramanathan	Springer Science & Business Media, 2006
2	Writing Testbenches Using SystemVerilog	Janick Bergeron	Springer Science & Business Media, 2007

Department: M.Tech. (VLSI and Embedded systems)			**Semester:**	**2**
Subject: VLSI Signal Processing				
Subject Code:	**24VES251**	**L – T – P - C:**		**3 – 0 – 0–3**

Sl. No	Course Objectives
1	To understand the basics and representation of DSP algorithms
2	To have an insight of Data flow graphs and pipelining
3	To understand Fast FIR filters and Rank order Filters
4	To have an insight of Look ahead schemes and round off noise computation

Unit	Description	Hrs
I	**Introduction to Digital Signal Processing :** Linear System Theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR Filters and IIR Filters - Filter Realizations. Representation of DSP Algorithms - Block diagram-SFG-DFG.	8
II	**Iteration Bound, Pipelining and Parallel Processing of FIR Filter:** Iteration Bound: Data-Flow Graph Representations- Loop Bound and Iteration Bound- Algorithms for Computing Iteration Bound-LPM Algorithm, MCM algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters- Parallel Processing- Pipelining and Parallel Processing for Low Power.	8
III	**Fast Convolution and Arithmetic Strength Reduction in Filters :** Fast Convolution: Cook-Toom Algorithm, Modified Cook-Toom Algorithm. Design of Fast Convolution Algorithm by Inspection. Parallel FIR filters, Fast FIR algorithms, Two parallel and three parallel. Parallel architectures for Rank Order filters, Odd Even Merge sort architecture.	8
IV	**Pipelined and Parallel Recursive Filters:** Pipeline Interleaving in Digital Filters, Pipelining in 1st Order IIR Digital Filters, Pipelining in Higher, Order IIR Filters, Parallel Processing for IIR Filters and Problems.	8
V	**Scaling and Round off Noise:** Scaling and Round off Noise, State Variable Description of Digital Filters, Scaling and Round off Noise Computation, Sl.ow-Down Retiming and Pipelining.	7

Course Outcomes:

Course outcome	Descriptions At the end of the course, students will be able to
CO1	Restate the knowledge of DSP Basics and algorithms(L1)
CO2	Identify various pipelining and parallel processing techniques(L2)
CO3	Analyze various Fast FIR filters and Rank order Filters(L3)
CO4	Interpret various Look ahead schemes and round off noise computation(L2, L3)

Course Articulation Matrix

PO/PSO / CO	PO1	PO2	PO3
CO1	1	1	2
CO2	1	1	1
CO3	2		1
CO4	1	1	

Text Books:

Sl. No.	Title	Author	Volume and Year of Edition
1	VLSI Digital Signal processing, John-Wiley	K.K Parhi	2007/1st edition
2	Digital Signal Processors	B.Venkatramani, M.Bhaskar	Tata McGraw-Hill, 2002.

Reference Books:

Sl. No.	Title	Author	Volume and Year of Edition
1	Digital Signal Processing, Prentice Hall of India	John G.Proakis, Dimitris G.Manolakis	2015, 2nd edition
2	DSP Integrated Circuits	Lars Wanhammer	Academic press, New York, 1999.

Department: M.Tech. (VLSI and Embedded systems)		**Semester:**	2
Subject: Automotive Electronics			
Subject Code:	**24VES252**	**L – T – P - C:**	**4 – 0 – 0 – 4**

Sl. No	Course Objectives
1	Providing an overview of automotive network systems.
2	Exposing students to the aspects of design, development, application, and performance issues associated with automotive network systems.
3	Introducing students to various automotive networking protocols.
4	Developing skills to design and implement networking protocols in automotive systems.
5	Enhancing understanding of safety-critical applications using automotive networking protocols.

Unit	Description	Hrs
I	**Introduction to Automotive Networking and General Purpose Protocols:** Overview of data communication and networking – need for in-vehicle networking – layers of OSI reference model – multiplexing and de-multiplexing concepts – vehicle buses. Overview of general-purpose networks and protocols – Ethernet, TCP, UDP, IP. Protocol for Low Data Rate Applications and Time Triggered Protocol: LIN standard overview – workflow concept – applications – LIN protocol specification – signals	**7**
II	**Frame transfer** – frame types – schedule tables – task behavior model – network management – status management. Introduction to CAN open – TTCAN – Device Net – SAE J1939.	**8**
III	**Protocol for Medium Data Rate Applications**: Overview of CAN – fundamentals – message transfer – frame types – error handling – fault confinement – bit time requirements.	**8**
IV	**Protocol for Infotainment**: MOST – overview of data channels – control channel – synchronous channel – asynchronous channel – logical device model – functions – methods – properties – protocol basics – network section – data transport – blocks – frames – preamble – boundary descriptor.	**8**
V	**Protocols for Safety Critical Applications**: Flex Ray – introduction – network topology – ECUs and bus interfaces – controller host interface and protocol operation controls – media access control and frame and symbol processing – coding/decoding unit.	**8**

Course outcome:

Course outcome	Descriptions
CO1	Illustrate the basics of automotive networking and protocols.
CO2	Comprehend the general protocols and their usage in the automotive sector.
CO3	Design and implement CAN and LIN protocols for various automotive applications.
CO4	Understand and apply time-triggered, media-oriented, and safety-critical protocols in automotive systems.

Course Articulation Matrix:

PO/PSO CO	PO1	PO2	PO3
CO1	3	2	2
CO2	2	3	2
CO3	2	2	3
CO4	2	3	2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Automotive In-Vehicle Networks	J. Gabrielleen	John Wiley & Sons, Limited, 2016

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Bosch Automotive Networking	Robert Bosch	Bentley Publishers, 2007
2	In-Vehicle Networks	Society of Automotive Engineers	2015
3	Automotive Electronics Handbook	Ronald K. Jurgen	McGraw-Hill Inc., 1999
4	Communication Networks: Fundamental Concepts and Key Architectures	Indra Widjaja, Alberto Leon-Garcia	McGraw-Hill College, 1st edition, 2000

Department: Electronics and Communication Engineering		**Semester:**	**II**
Subject: Intelligent IoT System Design and Architecture			
Subject Code:	24VES253	**L – T – P - C:**	**3-0-0-3**

Sl. No	Course Objectives
1.	Introduce the fundamentals, evolution, and enabling technologies of IoT.
2.	Understand IoT architectures, communication models, and security through case studies.
3.	Explore edge computing, cloud computing, real-time data management, and machine learning integration in IoT systems.
4.	Examine advanced IoT topics, including architectures, standards, and applications in smart cities, healthcare, and Industry 4.0

Unit	Description	Hrs
I	**Unit I: Introduction to IoT** Evolution of IoT, IoT Characteristics, IoT Enabling Technologies, Planning for an IoT Solution, IoT Use Case Development: Needs and Goals.(Text1: Chapters 1-3)	**8**
II	**Unit II: IoT Architecture and Design** IoT Architecture Reference Model, Functional Blocks of IoT, Communication Models, Security Models, Case Studies. (Text1:Chapters 2-5)	**8**
III	**Unit III: Computing in IoT** Edge Computing for IoT, Cloud Computing for IoT, Data Management in IoT, Real-Time Processing, Case Studies. (Text1:Chapters 5-6)	**8**
IV	**Unit IV: Machine Learning and Analytics in IoT** Introduction to Machine Learning for IoT, Data Analytics in IoT, Integration of ML Models, Predictive Analytics, Case Studies. (Text1:Chapter 7)	**8**
V	**Unit V: Advanced Topics and Applications** Service-Oriented Architecture, Event-Driven Architecture, IoT Standards, Applications in Smart Cities, Healthcare, and Industry 4.0, Future Trends and Re-search Directions. (Text1:Chapter 8)	**7**

Course Outcomes:

Course outcome	Descriptions
CO1	Understand the fundamental architecture of IoT systems.
CO2	Design and implement intelligent IoT solutions, integrating machine learning models for data analysis.
CO3	Utilize edge and cloud computing effectively in IoT projects.
CO4	Address security and privacy concerns in IoT design.

Course Articulation Matrix:

PO/PSO CO	PO1	PO2	PO3
CO1	1	-	-
CO2	3	2	-
CO3	3	2	2
CO4	3	2	3

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1.	Internet of Things: A Hands-On Approach	ArshdeepBahga, Vijay Madisetti	1st Edition, 2014
2.	Architecting the Internet of Things	Dieter Uckelmann, Mark Harrison, Florian Michahelles	1st Edition, 2011

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1.	Edge Computing: From Hype to Reality	Fadi Al-Turjman	1st Edition, 2018
2.	Fog and Edge Computing: Principles and Paradigms	RajkumarBuyya, SatishNarayanaSrirama	1st Edition, 2019
3.	Building the Internet of Things	MaciejKranz	1st Edition, 2016
4.	Internet of Things: Architecture and Design Principles	Raj Kamal	1st Edition, 2017

SRI SIDDHARTHA INSTITUTE OF TECHNOLOGY- TUMAKURU
(A constituent College of Siddhartha Academy of Higher Education, Tumakuru)
Academic year 2024-2025

Department: M.Tech. (VLSI and Embedded systems)	Semester:	II

Subject:	**VLSI TESTING**			
Subject Code:	**24VES254**		**L – T – P - C:**	**3 – 0 – 0 – 3**

Sl. No	Course Objectives
1	Understand the various benefits involved in VLSI Testing.
2	Apply the concepts of testing and fault modeling
3	Understand the concepts related to advanced design for testability and fault diagnosis.
4	Apply the concepts of Fault Diagnosis for Combinational Circuits

Unit	Description	Hrs
I	**UNIT I : Basics of testing and fault modelling:** Introduction to Testing - Faults in digital circuits - Modelling of faults - Logical Fault Models – Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.	8
II	**UNIT II : Test generation for combinational and Sequential Circuit:** Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.	**8**
III	**UNIT III : Design for testability:** Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches.	8
IV	**UNIT IV : Self-test and test algorithms:** Built-InSelf Test - Test pattern generation for BIST - Circular BIST - BIST Architectures – Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.	8
V	**UNIT V : Fault Diagnosis:** Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.	7

Course Outcomes:

Course outcome	Descriptions
CO1	Interpret the different challenges involved in VLSI Testing and Fault Modeling.(L2).
CO2	Explain various design for testability and self test and test algorithm.(L2).
CO3	Explain the design concepts of fault diagnosis.(L2).
CO4	Infer and discuss various design issues of self checking device(L3)

Course Articulation Matrix

PO/PSO / CO	PO1	PO2	PO3
CO1	3		3
CO2	3		3
CO3	3		3
CO4	3		3

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Digital Systems and Testable Design	M. Abramovici, M.A. Breuer and A.D. Friedman,	Jaico Publishing House.
2	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits	M.L. Bushnell and V.D. Agrawal,	Kluwer Academic Publishers.

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Design Test for Digital IC's and Embedded Core Systems	A.L. Crouch	Prentice Hall International.
2	Digital Circuit Testing and Testability	P.K. Lala	Academic Press, 2002.

Department: ECE			**Semester:**	**II**
Subject: Low Power VLSI Design				
Subject Code:	**24VES261**		**L – T – P - C:**	**3-0-0-3**

Sl. No	Course Objectives
1	To summarize the power optimization and trade off in digital circuits.
2	To illustrate the power estimation at different abstract levels.
3	To classify the general purpose and special techniques for low power system design.
4	To learn software co design in low power design

Unit	Description	Hrs
I	**Introduction to Low Power VLSI design and Analysis:** Introduction to low power VLSI design, Need for low power, Charging and Discharging Capacitance, Short-Circuit Current in CMOS, CMOS leakage current, Static current, Basic principles of low power design.	**08**
II	**Simulation and Probabilistic Power Analysis**: Spice Circuit Simulation, Discrete Transistor Modeling and Analysis, Gate level Logic Simulation, Architecture level Analysis, Probabilistic Power Analysis-Random logic signal, probability and frequency, power analysis techniques, signal entropy.	**08**
III	**Circuit level and Logic level design techniques:** Circuit, transistor and gate sizing, pin ordering, network restructuring and reorganization, adjustable threshold voltages, logic-Gate reorganization, signal gating, logic encoding,Pre-computation logic.	**08**
IV	**Special low power VLSI design techniques:** Power reduction in clock networks, CMOS floating node, Delay balancing, Switching activity reduction, parallel architecture voltage reduction.	**08**
V	**Software design and Power estimation:** Low power circuit design style, Sources of Software Power Dissipation, Software power estimation, Co-design for low power.	**07**

Course Outcomes:

Course outcome	Descriptions
CO1	Analyze the need for low power design and different sources of power dissipation in CMOS circuits. (L2)
CO2	Apply the different power optimization technique at various levels of abstraction. (L3)
CO3	Identify and apply the special techniques for low power applications. (L1, L3)
CO4	To get familiar with software co design for low power designs. (L2)

Course Articulation Matrix

CO \ PO	PO1	PO2	PO3
CO1			2
CO2	3		
CO3	1		3
CO4	1		2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Practical Low Power Digital VLSI Design	Gary Yeap	Springer US, Kluwer Academic Publishers, 2013.
2	Low power CMOS VLSI circuit design	Kaushik Roy, Sharat C. Prasad	Wiley Inter science Publications",2013. 21

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Low Voltage Low Power VLSI Subsystems	Kiat-Seng Yeo, Kaushik Roy	Tata Mc-Graw Hill, 2015.

Department: M.Tech. (VLSI and Embedded systems)		**Semester:**	**2**
Subject: MICRO ELECTRO MECHANICAL SYSTEMS (MEMS)			
Subject Code:	**24VES262**	**L – T – P - C:**	**3 – 0 – 0–3**

Sl. No	Course Objectives
1	To familiarize with MEMS Materials and Scaling Laws in Miniaturation.
2	To revive various concepts of Engineering Mechanics and Thermo fluid Engineering for Microsystems Design. Also study the Microsystems Fabrication Process.
3	To familiarize with Microsystems Design, Assembly and Packaging.
4	To explore on various Case Study of MEMS Devices.

Unit	Description	Hrs
I	**Overview of MEMS and Microsystems, Mems Materials and Scaling Laws in Miniaturization:** Microsystems and microelectronics, Microsystems and miniaturization, Working principle of micro system - Micro sensors, Micro actuators, MEMS with Micro actuators. Materials for MEMS - Substrate & wafer, Si as a substrate material, Si compound, Si Piezo-resistors, polymers packaging Materials. Scaling Laws in Miniaturization-Scaling in Geometry, scaling in Electrostatic Forces, scaling in Electromagnetic Forces, scaling in Electricity.	8
II	**Engineering Mechanics and Thermofluidic Engineering for Microsystems Design:** Atomic structure of matter, Ions and ionization, Molecular theory of matter and intermolecular forces, Diffusion process, Plasma physics, Thermo mechanical analysis, Overview of finite element analysis. Thermo fluid Engineering-Characteristics of Moving Fluids, The Continuity Equation, The Momentum Equation.	8
III	**Microsystems Fabrication Process:** Fabrication Process - Photolithography, Ion implantation, Oxidation, Chemical vapor deposition (CVD), Physical vapor deposition, Deposition by Epitaxy, Etching. Manufacturing Process - Bulk Micromachining, Surface Micromachining and LIGA Process.	8
IV	**Microsystems Design, Assembly and Packaging:** Micro system Design - Design consideration, process design, Mechanical design using MEMS. Mechanical packaging of Microsystems, interfacings in Microsystems packaging, packaging technology, selection of packaging materials.	8
V	**Case Study of Mems Devices:** Case study on strain sensors, Temperature sensors, Pressure sensors, Humidity sensors, Accelerometers, Gyroscopes, RF MEMS Switch, phase shifter, and smart sensors. Case study of MEMS pressure sensor Packaging.	7

Course Outcomes:

Course outcome	Descriptions
CO1	Understand the fundamentals of MEMS and its Design methodology. (L1)
CO2	Compare various Mechanical & Electronics Sensors and its applications. (L2)
CO3	Analyze various bonding and packaging techniques in MEMS(L3).
CO4	Interpret the scaling issues in MEMS. (L2)

Course Articulation Matrix:

PO/PSO / CO	PO1	PO2	PO3
CO1	3		
CO2		2	
CO3	1		
CO4			2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	MEMS and Microsystems: design , manufacture, and nanoscale Engineering	Tai-Ran Hsu, John Wiley and Sons, Inc., Hoboken	New Jersey, 2008. 2nd Edition.
2	Foundations of MEMS	Chang Liu	Pearson Indian Print, 1st Edition, 2012.

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	RF MEMS - Theory Design and Technology	Gabriel M Rebeiz	John Wiley & Sons, 2004.
2	Micro sensors MEMS and smart devices	Julian W Gardner	John Wiley and sons Ltd, 2001.

Department: M.Tech. (VLSI and Embedded systems)			**Semester:**	**2**
Subject: Electromagnetic Interference and Compatibility				
Subject Code:	**24VES263**	**L – T – P - C:**		**3 – 0 – 0 –3**

Sl. No	Course Objectives
1	Familiarize with the fundamentals that are essential for electronics industry in the field of EMI / EMC
2	Understand EMI sources and its measurements.
3	Understand the various techniques for electromagnetic compatibility.
4	Acquire the Knowledge of EMI test methods & Instrumentation

Unit	Description	Hrs
I	Introduction to EMI and EMC, Intra and inter system EMI, Elements of Interference, Sources and Victims of EMI, Conducted and Radiated EMI emission and susceptibility, Case Histories, Radiation hazards to humans, Various issues of EMC, EMC Testing categories, EMC Engineering Application.	7
II	Sources of Electromagnetic noise, typical noise paths, modes of noise coupling, designing for EM compatibility, lightening discharge, electro static discharge (ESD), electromagnetic pulse (EMP).	7
III	Electromagnetic emissions, noise form relays and switches, non-linearities in circuits, passive inter modulation, transients in power supply lines, EMI from power electronic equipment, EMI as combination of radiation and conduction. Open area test sides: OATS measurements, measurement precautions.	8
IV	**EMI mitigation techniques:** Working principle of Shielding, LF Magnetic shielding, Apertures and shielding effectiveness, Choice of Materials for H, E, and free space fields, Gasketing and sealing, PCB Level shielding, Principle of Grounding, Isolated grounds, Grounding strategies for Large systems, Grounding for mixed signal systems, Electrical bonding, Filter types and operation, Surge protection devices, Transient protection.	9
V	**EMI test methods and instrumentation:** EMI Shielding effectiveness tests, TEM cell for immunity test, Shielded chamber , Shielded anechoic chamber, EMI test receivers, Spectrum analyzer, EMI test wave simulators, EMI coupling networks, Line impedance stabilization networks, Feed through capacitors, Antennas, Current probes, MIL -STD test methods, Civilian STD test methods.	9

Course Outcomes:

Course outcome	Descriptions
CO1	Identify the various types and mechanisms of Electromagnetic Interference. (L2)
CO2	Real-world EMC design constraints and make appropriate tradeoffs to achieve the most cost-effective design that meets all requirements.(L2)
CO3	Designing electronic systems that function without errors or problems related to electromagnetic compatibility. (L3)
CO4	Diagnose and solve basic electromagnetic compatibility problems.(L3)

Course Articulation Matrix

CO \ PO	PO1	PO2	PO3
CO1	3	3	
CO2	2	3	
CO3	2	3	2
CO4	2	3	2

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Introduction to Electromagnetic Compatibility	Clayton Paul	Wiley Interscience, 2006.
2	Engineering Electromagnetic Compatibility	V Prasad Kodali	IEEE Press, Newyork, 2001.
3	An ASIC Low Power Primer	Rakesh Chadha, Bhasker J	Springer, ISBN: 978-1-4614-1119-2. 2011

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Electromagnetic Compatibility Engineering	Henry W. Ott	John Wiley & Sons Inc, Newyork, 2009.
2	Electromagnetic Interference and Compatibility		IMPACT series, IIT-Delhi, Modules1-9.

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Academic year 2024-2025

Department: ECE(VES)	Semester:	II

Subject: VLSI System on chip				
Subject Code:	24VES264		L – T – P - C:	3 – 0 – 0 -- 3

Sl. No	Course Objectives
1	Learn the various benefits involved in SoC design and typical design goals related to SoC design.
2	Apply the concepts of embedded memories with interconnect architectures for SoC design.
3	Understand the concepts related to SoC design flow, co-design and various power management issues.

Unit	Description	Hrs
I	**Motivation for SoC Design** Review of Moore's law and CMOS scaling, benefits of System-on-Chip integration in terms of cost, power, and performance, comparison of System- on-Board, System-on-Chip and System-in-Package, typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization, productivity gap issues and the ways to improve the gap – IP based design and design reuse.	08
II	**Embedded Processors** Microprocessors, Microcontrollers, DSP and their selection criteria, review of RISC and CISC instruction sets, Von-Neumann and Harward architectures and interrupt architectures	08
III	**Embedded Memories** Scratchpad memories, Cache memories, Flash memories, Embedded DRAM, topics related to cache memories, Cache coherence, MESI protocol.	08
IV	**Interconnect architectures for SoC** Bus architecture and its limitations, Network on Chip (NoC) topologies, packet switching and circuit switching, routing algorithms, static and dynamic routing, distributed and source routing, minimal and non-minimal routing, flow control, quality of service and NoC architectures .	08
V	**CASE STUDIES** 1.T. N. Tan, P. Duong-Ngoc, T. X. Pham and H. Lee, "Novel Performance Evaluation Approach of AMBA AXI-Based SoC Design," *2021 18th International SoC Design Conference (ISOCC)*, Jeju Island, Korea, Republic of, 2021, pp. 403-404, doi: 10.1109/ISOCC53507.2021.9613920. 2. J. Yue, W. Sun, H. Yang and Y. Liu, "Challenges and Opportunities of Energy-Efficient CIM SoC Design for Edge AI Devices," *2021 18th International SoC Design Conference (ISOCC)*, Jeju Island, Korea, Republic of, 2021, pp. 197-198, doi: 10.1109/ISOCC53507.2021.9613846. 3.K. Kang *et al*., "Seamless SoC Verification Using Virtual Platforms: An Industrial Case Study," *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Florence, Italy, 2019, pp. 1204-1205, doi: 10.23919/DATE.2019.8715128. 4. B. Khailany *et al*., "INVITED: A Modular Digital VLSI Flow for High-Productivity SoC Design," *2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, 2018, pp. 1-6, doi: 10.1109/DAC.2018.8465897.	08

Course Outcomes:

Course outcome	Descriptions
CO1	Interpret the different challenges involved in design of SoC and compare different design configurations such as System-on-Board and System-in-Package and case studies related to soc design.(L2).
CO2	Explain various embedded processors, memory architectures and hardware accelerators related to SoC design.(L2).
CO3	Infer NOC with mixed signal components(L3).
CO4	Analyse the performance of various NoC architecture (L4).

Course Articulation Matrix

PO/PSO / CO	PO1	PO2	PO3
CO1	3		3
CO2	2		2
CO3	3		3
CO4	3		3

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1.	On-Chip Communication Architectures: System on Chip Interconnect	Sudeep Pasricha and NikilDutt	Morgan Kaufmann Publishers © 2008
2.	Networks on Chips: Technology and Tools	Luca Benini and Giovanni De Micheli	Morgan Kaufmann Publishers © 2006
3.	Embedded Systems: A Contemporary Design Tool	James K. Peckol	Wiley Student Edition, 2007.

Reference Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Introduction to system on package sop- Miniaturization of the entire System	Rao R. Tummala, MadhavanSwamina than	McGraw-Hill-2008
2	Transaction Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems	Frank Ghenassia	Springer © 2005
3	Surviving the SOC revolution: a guide to platform-based design	Henry Chang	Kluwer (Springer), 1999

Department M.Tech. (VLSI and Embedded systems)			**Semester:**	**2**
Subject: VLSI DESIGN AND ADVANCED EMBEDDED SYSTEMS LAB				
Subject Code:	**24VESLB2**	**L – T – P - C:**		**0 – 0 – 3–1.5**

Sl. No	Course Objectives
1	Providing knowledge about interconnects, stick diagrams and layout.
2	To impart knowledge about the DC analysis, timing analysis, in combinational and sequential circuits.
3	To provide hands-on experience in designing and implementing advanced embedded systems using micro controllers.
4	To develop proficiency in programming various interfaces and protocols commonly used in embedded systems, such as UART, I2C, PWM, Watchdog timer, and Real-Time Clock (RTC) using LPC2148.

Sl No	Programme/ Experiment
1	Realize a Inverter & Buffer in CMOS and verify its truth table in both schematic and layout. i) Plot voltage v/s time and voltage v/s voltage. ii) Show the 3D and 2D view for the layout. iii) Change the technology without changing the layout and simulate rise and fall time. iv) Verify the design rule check (DRC).
2	Realize a two input NAND & AND gate in CMOS and verify its truth table in both schematic and layout. i) Plot voltage v/s time and voltage v/s voltage. ii) Show the 3D and 2D view for the layout. iii) Change the technology without changing the layout and simulate rise and fall time. iv) Verify the design rule check (DRC).
3	Realize a two input NOR & OR gate in CMOS and verify its truth table in both schematic and layout. i) Plot voltage v/s time and voltage v/s voltage. ii) Show the 3D and 2D view for the layout. iii) Change the technology without changing the layout and simulate rise and fall time. iv) Verify the design rule check (DRC).
4	Implement a clocked D, SR flip- flop with preset and clear and verify its timing diagram in both schematic and layout. i) Make Verilog file of the schematic and generate the layout. ii)Show the 3D and 2D view for the layout. iii) Plot the voltage v/s time.
5	Implement a 3 bit Asynchronous counter in both schematic and layout for specific technology. i) Make Verilog file of the schematic and generate the layout. ii) Show the 3D and 2D view for the layout. iii) Plot voltage v/s time and voltage v/s voltage.

6	Program to send and receive data via UART using LPC2148.
7	Program to interface an EEPROM using I2C protocol.
8	Program to generate PWM signals using LPC2148.
9	Program to configure and use the Watchdog timer.
10	Program to interface and read the Real-Time Clock (RTC) using LPC2148.

Course Outcomes:

Course outcome	Descriptions
CO1	Design CMOS schematics and layouts for Basic Gates , Universal Gates, Combinational circuits, Sequential Circuits and analog circuits with minimum number of transistors.
CO2	Synthesize the schematics, draw and generate the layouts using Microwind Tool. Also check and verify parasitic extraction, design rules and simulation.
CO3	Develop embedded systems with LPC2148, implementing various interfaces and protocols such as UART, I2C.
CO4	Develop proficiency in designing and implementing advanced embedded systems using microcontrollers, including programming various interfaces such as PWM, Watchdog timer, and Real-Time Clock (RTC) using LPC2148

Course Articulation Matrix:

PO/PSO / CO	PO1	PO2	PO3
CO1	3		
CO2		1	
CO3			1
CO4	1		

Text Books:

Sl. No.	Title	Authors	Volume and Year of Edition
1	Digital VLSI Chip Design with Cadence and Synopsys CAD Tools	Erik Brunvand	Addison-Wesley, 1st Edition, 2019
2	Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C	Daniel W. Lewis	Morgan Kaufmann, 2015

REFERENCES:

1. www.microwind.net

2. ieee-projects.skiveprojects.com/technology-vlsi-domain-microwind

3.intranet-gei.insa-toulouse.fr/~sicard/microwind/students.html

LIST OF MICROWIND RELATED PROJECTS:

1.Analysis and on chip monitoring of gate oxide breakdown in sram cells.
2.A reconfigurable clock polarity assignment flow for clock gated designs.
3.Energy efficient low latency 600 mhz fir with high overdrive charge recovery logic.
4.Investigating the impact of logic and circuit implementation on full adder performance.
5.A low power single phase clock multiband flexible divider.
6.Radio frequency circuit.

LIST OF VLSI COMPANY WEBSITES

1.http://vimalzalariya.blogspot.in/2012/07/list-of-vlsi-companies120.html
2.http://www.vlsiworld.com/component/option,com_glossary/func,display/letter,/page,1/catid,30/Itemid,44/
3.https://sreejinair.wordpress.com/vlsi-companies-in-india/
4.http://bhavitkaushik.blogspot.in/2015/05/list-of-vlsi-companies-in-india.html
5.http://www.vlsiencyclopedia.com/2011/12/list-of-vlsi-companies.html
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